DDR2 SDRAM SODIMM

MT16HTS25664H – 2GB[1]

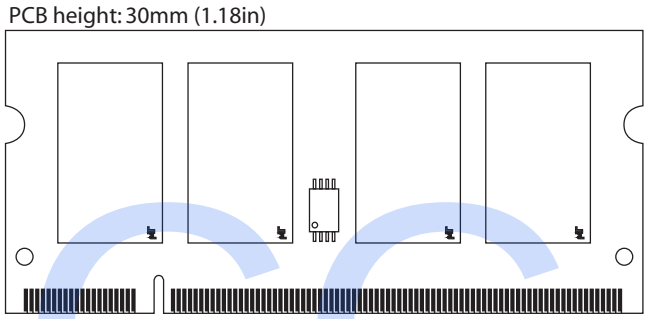
MT16HTS51264H – 4GB

For component specifications, refer to Micron's Web site: www.micron.com

Features

- 200-pin, small outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, or PC2-5300
- 2GB (256 Meg x 64) and 4GB (512 Meg x 64)
- $V_{DD} = V_{DDQ} = +1.8V$
- $V_{DDSPD} = +1.7V$ to $+3.6V$
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths (BL) 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts
- Dual rank, TwinDie™ (2COB) DRAM devices

Figure 1: 200-Pin SODIMM (MO-224 R/C D)



Options	Marking
• Operating temperature[2]	
– Commercial (0°C ≤ T_A ≤ +70°C)	None
– Industrial (–40°C ≤ T_A ≤ +85°C)	I
• Package	
– 200-pin DIMM (Pb-free)	Y
• Frequency/CAS latency	
– 2.5ns @ CL 6 (DDR2-800)	-800
– 3.0ns @ CL = 5 (DDR2-667)	-667
– 3.75ns @ CL = 4 (DDR2-533)	-53E
– 5.0ns @ CL = 3 (DDR2-400)[3]	-40E

Notes: 1. End of life.
2. Contact Micron for industrial temperature module offerings.
3. Not recommended for new designs.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-800	PC2-6400	800	667	533	–	15	15	55
-667	PC2-5300	667	667	533	400	15	15	55
-53E	PC2-4200	–	–	533	400	15	15	55
-40E	PC2-3200	–	–	400	400	15	15	55

Table 2: Addressing

Parameter	2GB	4GB
Refresh count	8K	8K
Row address	16K (A0–A13)	32K (A0–A14)
Device bank address	8 (BA0–BA2)	8 (BA0–BA2)
Device configuration	2Gb TwinDie (128 Meg x 8)	4Gb TwinDie (256 Meg x 8)
Column address	1K (A0–A9)	1K (A0–A9)
Module rank address	2 (S0#, S1#)	2 (S0#, S1#)

Table 3: Part Numbers and Timing Parameters – 2GB

Base device: MT47H256M8THJ,[1] 2Gb TwinDie DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT16HTS25664HY-800__	2GB	256 Meg x 64	6.4 GB/s	2.5ns/800MT/s	6-6-6
MT16HTS25664HY-667__	2GB	256 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT16HTS25664HY-53E__	2GB	256 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT16HTS25664HY-40E__	2GB	256 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Table 4: Part Numbers and Timing Parameters – 4GB

Base device: MT47H512M8THM,[1] 4Gb TwinDie DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT16HTS51264HY-800__	4GB	512 Meg x 64	6.4 GB/s	2.5ns/800MT/s	6-6-6
MT16HTS51264HY-667__	4GB	512 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT16HTS51264HY-53E__	4GB	512 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4

Notes: 1. Data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes.
Example: MT16HTS51264HY-667A1.

Pin Assignments and Descriptions

Table 5: Pin Assignments

200-Pin SODIMM Front								200-Pin SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REF}	51	DQS2	101	A1	151	DQ42	2	V_{SS}	52	DM2	102	A0	152	DQ46
3	V_{SS}	53	V_{SS}	103	V_{DD}	153	DQ43	4	DQ4	54	V_{SS}	104	V_{DD}	154	DQ47
5	DQ0	55	DQ18	105	A10	155	V_{SS}	6	DQ5	56	DQ22	106	BA1	156	V_{SS}
7	DQ1	57	DQ19	107	BA0	157	DQ48	8	V_{SS}	58	DQ23	108	RAS#	158	DQ52
9	V_{SS}	59	V_{SS}	109	WE#	159	DQ49	10	DM0	60	V_{SS}	110	S0#	160	DQ53
11	DQS0#	61	DQ24	111	V_{DD}	161	V_{SS}	12	V_{SS}	62	DQ28	112	V_{DD}	162	V_{SS}
13	DQS0	63	DQ25	113	CAS#	163	NC	14	DQ6	64	DQ29	114	ODT0	164	CK1
15	V_{SS}	65	V_{SS}	115	S1#	165	V_{SS}	16	DQ7	66	V_{SS}	116	A13	166	CK1#
17	DQ2	67	DM3	117	V_{DD}	167	DQS6#	18	V_{SS}	68	DQS3#	118	V_{DD}	168	V_{SS}
19	DQ3	69	NC	119	ODT1	169	DQS6	20	DQ12	70	DQS3	120	NC	170	DM6
21	V_{SS}	71	V_{SS}	121	V_{SS}	171	V_{SS}	22	DQ13	72	V_{SS}	122	V_{SS}	172	V_{SS}
23	DQ8	73	DQ26	123	DQ32	173	DQ50	24	V_{SS}	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51	26	DM1	76	DQ31	126	DQ37	176	DQ55
27	V_{SS}	77	V_{SS}	127	V_{SS}	177	V_{SS}	28	V_{SS}	78	V_{SS}	128	V_{SS}	178	V_{SS}
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56	30	CK0	80	CKE1	130	DM4	180	DQ60
31	DQS1	81	V_{DD}	131	DQS4	181	DQ57	32	CK0#	82	V_{DD}	132	V_{SS}	182	DQ61
33	V_{SS}	83	NC	133	V_{SS}	183	V_{SS}	34	V_{SS}	84	NC	134	DQ38	184	V_{SS}
35	DQ10	85	BA2	135	DQ34	185	DM7	36	DQ14	86[1]	NC/A14	136	DQ39	186	DQS7#
37	DQ11	87	V_{DD}	137	DQ35	187	V_{SS}	38	DQ15	88	V_{DD}	138	V_{SS}	188	DQS7
39	V_{SS}	89	A12	139	V_{SS}	189	DQ58	40	V_{SS}	90	A11	140	DQ44	190	V_{SS}
41	V_{SS}	91	A9	141	DQ40	191	DQ59	42	V_{SS}	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	V_{SS}	44	DQ20	94	A6	144	V_{SS}	194	DQ63
45	DQ17	95	V_{DD}	145	V_{SS}	195	SDA	46	DQ21	96	V_{DD}	146	DQS5#	196	V_{SS}
47	V_{SS}	97	A5	147	DM5	197	SCL	48	V_{SS}	98	A4	148	DQS5	198	SA0
49	DQS2#	99	A3	149	V_{SS}	199	V_{DDSPD}	50	NC	100	A2	150	V_{SS}	200	SA1

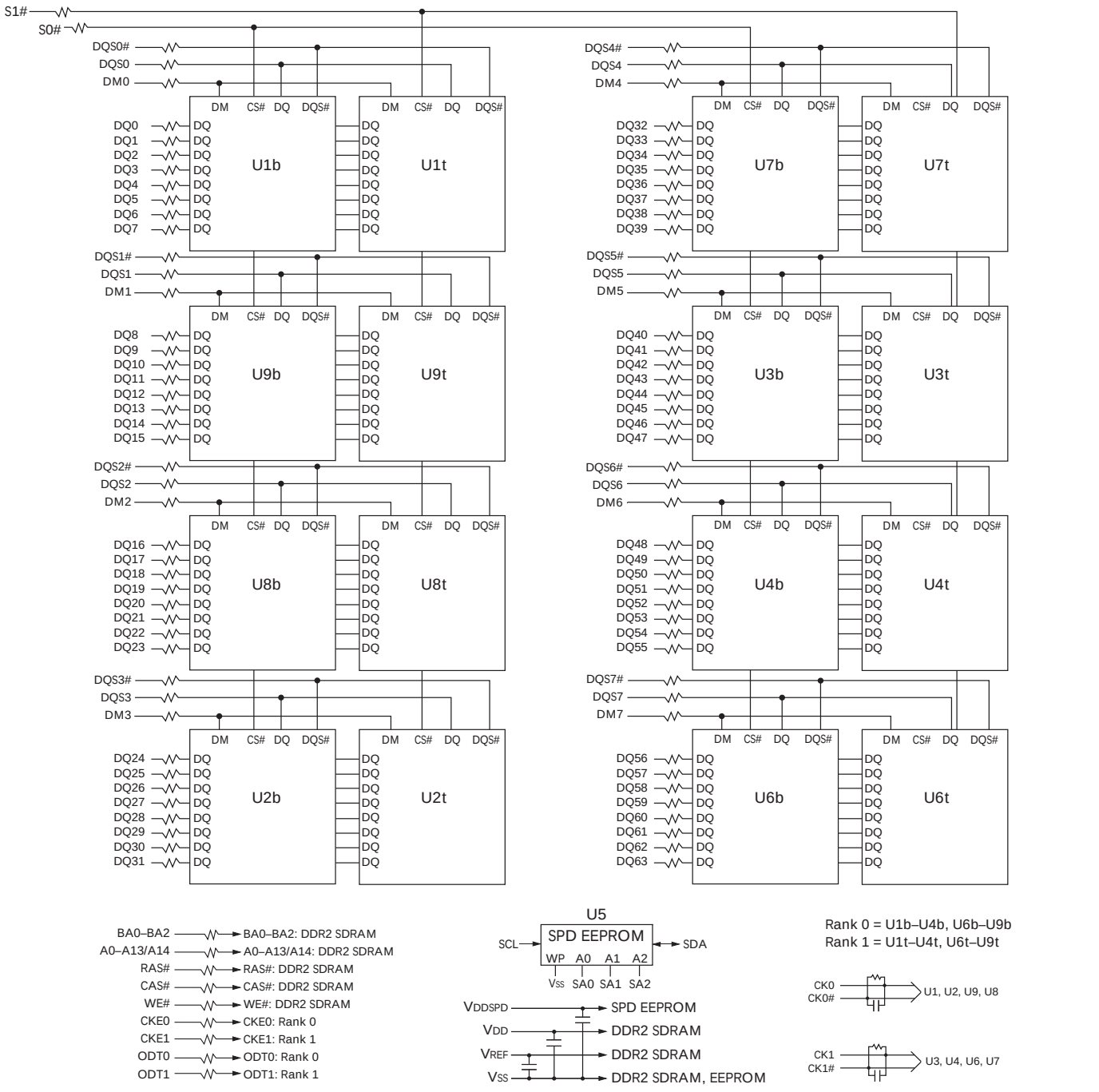
Notes: 1. Pin 86 is NC for 2GB and A14 for 4GB.

Table 6: Pin Descriptions

Symbol	Type	Description
A0–A14	Input (SSTL_18)	**Address inputs:** Provide the row address for ACTIVE commands and the column address, and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. A0–A13 (2GB) and A0–A14 (4GB).
BA0–BA2	Input (SSTL_18)	**Bank address inputs:** BA0–BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
CK0, CK0# CK1, CK1#	Input (SSTL_18)	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0, CKE1	Input (SSTL_18)	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
DM0–DM7	Input (SSTL_18)	**Data input mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
ODT0, ODT1	Input (SSTL_18)	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input (SSTL_18)	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
S0#, S1#	Input (SSTL_18)	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# provides for external rank selection on systems with multiple ranks. S# is considered part of the command code.
SA0–SA1	Input (SSTL_18)	**Presence-detect address inputs:** These pins are used to configure the presence-detect devices.
SCL	Input (SSTL_18)	**Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module.
DQ0–DQ63	I/O (SSTL_18)	**Data input/output:** Bidirectional data bus.
DQS0–DQS7, DQS0#–DQS7#	I/O (SSTL_18)	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
SDA	I/O (SSTL_18)	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
V_{DD}	Supply	**Power supply:** +1.8 ±0.1V.
V_{DDSPD}	Supply	**Serial EEPROM positive power supply:** +1.7V to +3.6V.
V_{REF}	Supply	SSTL_18 reference voltage ($V_{DD/2}$).
V_{SS}	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.

Functional Block Diagram

Figure 2: Functional Block Diagram



General Description

The MT16HTS25664H and MT16HTS51264H DDR2 SDRAM modules are high-speed, CMOS, dynamic random access 2GB and 4GB memory modules organized in a x64 configuration. These modules use 2Gb and 4Gb TwinDie DDR2 SDRAM devices with eight internal banks.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (1:0), which provide four unique DIMM/EEPROM addresses. Write protect (WP) is pulled down to V_{SS} on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 7 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated on the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}		–1.0	+2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		–0.5	+2.3	V
II	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	Address inputs RAS#, CAS#, WE#	–80	+80	µA
		S#, CKE, ODT, CK, CK#	–40	+40	
		DM	–10	+10	
Ioz	Output leakage current; 0V ≤ V_{OUT}; DQ and ODT are disabled	DQ, DQS, DQS#	–10	+10	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = valid V_{REF} level		–32	+32	µA
T_A	Module ambient operating temperature	Commercial	0	+70	°C
		Industrial	–40	+85	°C
T_C[1]	DDR2 SDRAM component case operating temperature[2]	Commercial	0	+85	°C
		Industrial	–40	+95	°C

Notes: 1. The refresh rate is required to double when 85°C < T_C ≤ 95°C.
2. For further information, refer to technical note TN-00-08: “Thermal Applications,” available on Micron’s Web site.

Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations. JEDEC modules are currently designed using simulations to close timing budgets.

AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron’s Web site. Module speed grades correlate with component speed grades, as shown in Table 8.

Table 8: Module and Component Speed Grades

Module Speed Grade	Component Speed Grade
-800	-25
-667	-3
-53E	-37E
-40E	-53E

Table 9: DDR2 I_{DD} Specifications and Conditions – 2GB

Values are shown for the MT47H256M8THJ DDR2 SDRAM only and are computed from values specified in the 2Gb TwinDie (256 Meg x 8) component data sheet

Parameter/Condition		Symbol	-800	-667	-53E	-40E	Units
Operating one bank active-precharge current: $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRAS = ^tRASmin (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD0}	816	776	656	656	mA
Operating one bank active-read-precharge current: I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRAS = ^tRASmin (I_{DD})$, $^tRCD = ^tRCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I_{DD4W}		I_{DD1}	976	896	856	816	mA
Precharge power-down current: All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2P}	112	112	112	112	mA
Precharge quiet standby current: All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2Q}	456	376	376	336	mA
Precharge standby current: All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD2N}	496	416	416	376	mA
Active power-down current: All device banks open; $^tCK = ^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	I_{DD3PF}	296	296	296	296	mA
	Slow PDN exit MR[12] = 1	I_{DD3PS}	136	136	136	136	mA
Active standby current: All device banks open; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRASmax (I_{DD})$, $^tRP = ^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD3N}	576	536	456	416	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRASmax (I_{DD})$, $^tRP = ^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4W}	1376	1176	1096	936	mA
Operating burst read current: All device banks open; Continuous burst read; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRASmax (I_{DD})$, $^tRP = ^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4R}	1376	1176	1096	936	mA
Burst refresh current: $^tCK = ^tCK (I_{DD})$; REFRESH command at every $^tRFC (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD5}	1976	1816	1776	1736	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		I_{DD6}	112	112	112	112	mA
Operating bank interleave read current: All device banks interleaving reads; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = $^tRCD (I_{DD})$ - = 1 × $^tCK (I_{DD})$; $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRRD = ^tRRD (I_{DD})$, $^tRCD = ^tRCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching		I_{DD7}	2776	2336	2256	2176	mA

Table 10: DDR2 I_{DD} Specifications and Conditions – 4GB

Values are shown for the MT47H512M8THM DDR2 SDRAM only and are computed from values specified in the 4Gb TwinDie (512 Meg x 8) component data sheet

Parameter/Condition		Symbol	-800	-667	-53E	Units
Operating one bank active-precharge current: $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RC = {}^{t}RC (I_{DD})$, $^{t}RAS = {}^{t}RASmin (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD0}	TBD	904	824	mA
Operating one bank active-read-precharge current: I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RC = {}^{t}RC (I_{DD})$, $^{t}RAS = {}^{t}RASmin (I_{DD})$, $^{t}RCD = {}^{t}RCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I_{DD4W}		I_{DD1}	TBD	1264	944	mA
Precharge power-down current: All device banks idle; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2P}	TBD	128	128	mA
Precharge quiet standby current: All device banks idle; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2Q}	TBD	504	424	mA
Precharge standby current: All device banks idle; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD2N}	TBD	584	504	mA
Active power-down current: All device banks open; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	I_{DD3PF}	TBD	384	344	mA
	Slow PDN exit MR[12] = 1	I_{DD3PS}	TBD	144	144	mA
Active standby current: All device banks open; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RAS = {}^{t}RASmax (I_{DD})$, $^{t}RP = {}^{t}RP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD3N}	TBD	544	464	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RAS = {}^{t}RASmax (I_{DD})$, $^{t}RP = {}^{t}RP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4W}	TBD	1304	1144	mA
Operating burst read current: All device banks open; Continuous burst reads; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RAS = {}^{t}RASmax (I_{DD})$, $^{t}RP = {}^{t}RP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4R}	TBD	1464	1304	mA
Burst refresh current: $^{t}CK = {}^{t}CK (I_{DD})$; Refresh command at every $^{t}RFC (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD5}	TBD	2344	2184	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		I_{DD6}	TBD	128	128	mA
Operating bank interleave read current: All device banks interleaving reads; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = $^{t}RCD (I_{DD})$ - 1 × $^{t}CK (I_{DD})$; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RC = {}^{t}RC (I_{DD})$, $^{t}RRD = {}^{t}RRD (I_{DD})$, $^{t}RCD = {}^{t}RCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching		I_{DD7}	TBD	2824	2464	mA

Serial Presence-Detect

Table 11: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT}= 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3.0	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3.0	µA
Standby current	I_{SB}	1.6	4.0	µA
Power supply current, READ: SCL clock frequency = 100 kHz	I_{CCR}	0.4	1.0	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	I_{CCW}	2.0	3.0	mA

Table 12: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
Data-out hold time	^{t}DH	200	–	ns	
SDA and SCL fall time	^{t}F	–	300	ns	2
Data-in hold time	$^{t}HD:DAT$	0	–	µs	
Start condition hold time	$^{t}HD:STA$	0.6	–	µs	
Clock HIGH period	$^{t}HIGH$	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I	–	50	ns	
Clock LOW period	^{t}LOW	1.3	–	µs	
SDA and SCL rise time	^{t}R	–	0.3	µs	2
SCL clock frequency	^{f}SCL	–	400	kHz	
Data-in setup time	$^{t}SU:DAT$	100	–	ns	
Start condition setup time	$^{t}SU:STA$	0.6	–	µs	3
Stop condition setup time	$^{t}SU:STO$	0.6	–	µs	
WRITE cycle time	^{t}WRC	–	10	ms	4

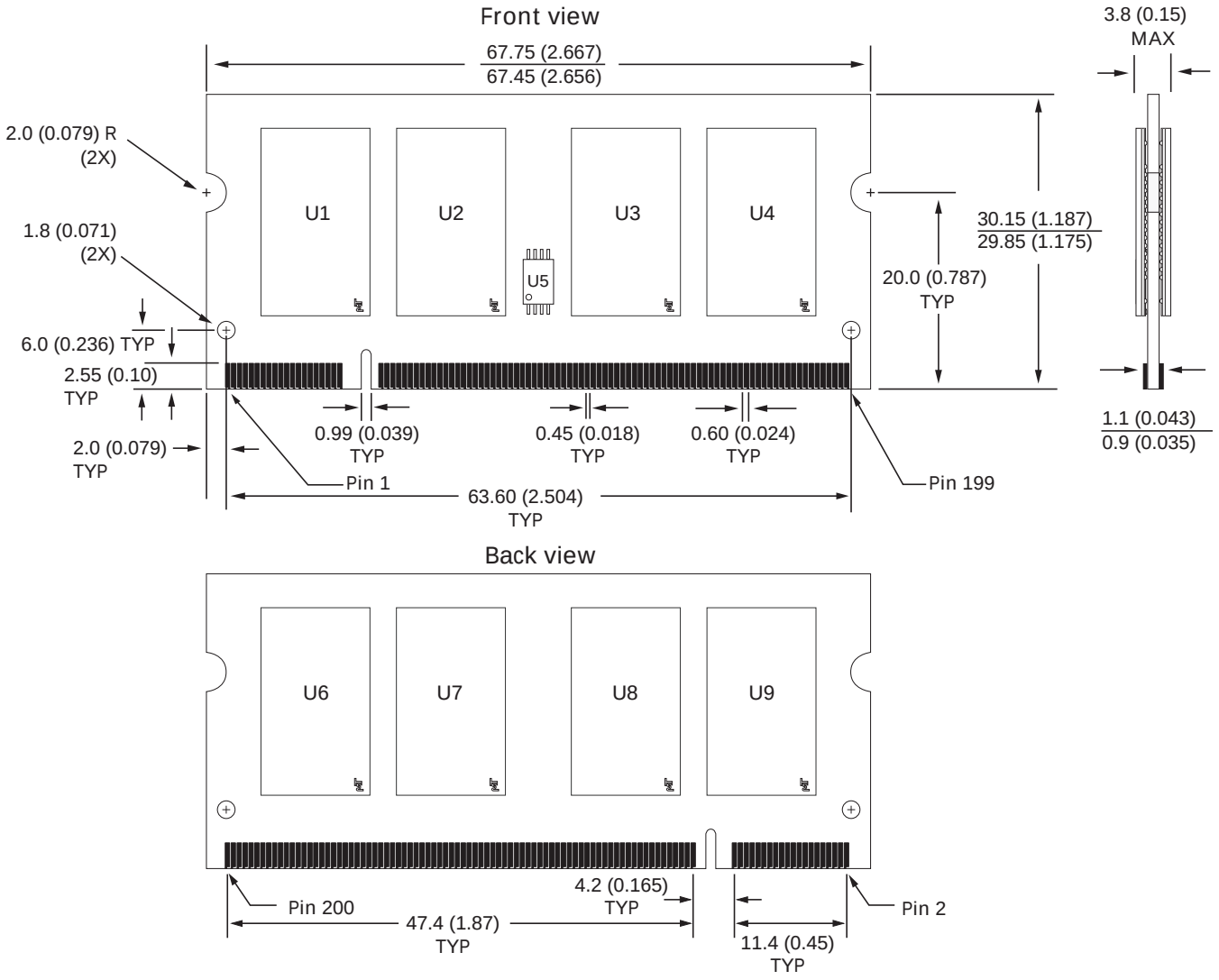
Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

Module Dimensions

Figure 3: 200-Pin DDR2 SODIMM



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or TYP where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

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Revision History

Rev. D 5/09

- "Features" on page 1: Added PC2-6400 to data transfer rates.
- Published externally.

Rev. C 4/09

- Added -800 speed grade.
- Not published externally — customer draft only.

Rev. B 10/07

- Updated file name from HTS16C256x64H.fm to HTS16C256_512x64H.fm.
- Added 4GB – MT16HTS51264H.
- Updated to latest format and data diet.
- Added note "Not recommended for new designs" for MT16HTS25664H – 2GB.
- Updated the I_{DD} tables.
- Removed the SPD matrices and replaced them with a link to the online SPD Web site.
- Referenced PCB 0402 in this revision.
- Removed part number MT16HTS51264HY-40E from Table 4 on page 2.

Rev. A, Released (No Mark) 04/06

- Initial release.