**DESCRIPTION**

The S1R72013 is a general-purpose device controller LSI that supports the USB2.0-compliant high/full-speed modes.

With the field-proven, UTMI Rev.1.0 specification-compliant transceiver circuit, it assures connectivity of USB devices. It realizes reduction of the number of pins and speed-up of the DMA on the basis of the S1R72003 with the field-proven as the USB2.0 device controller.

Moreover, the PFBGA packages are lined up as the mass production model for the world first USB2.0 device controller.

**FEATURES**

- Supports HS (480Mbps) and FS (12Mbps) transfer modes.
- Has built-in HS/FS termination.
- Supports Control, Bulk, and Interrupt transfers.
- Supports three general-purpose Endpoints and Endpoint 0.
- Has a built-in 2.5KB programmable FIFO for Endpoint use.
- Incorporates general-purpose DMA ports of 8/16-bit width (*1).
  - Capable of operating as general-purpose non-synchronous multiword/general-purpose non-synchronous singleword/synchronous DMA sleeve.
  - 30Mword/s high-speed/burst transfers.
- Installed with 8-bit width (*1) general CPU Interface
- Supports H/W protocol
  - Auto Speed Negotiation, Descriptor return, etc.
- Has built-in oscillation circuit (Supports f = 12MHz/24MHz crystal oscillator)
- Uses multiple power management mode
- Runs on a single 3.3V power supply
- Uses 5.0V tolerant cells for Vbus, CPU Interface, and DMA port input pins.
- QFP13-64pin package, PFBGA-100pin package

(*1) When using the DMA with 16-bit width, share with the bus. The register access is always 8-bit width.
CIRCUIT EXAMPLES

8bit CPU Bus

Data Processing ASIC

General CPU

USB Interface

S1R72013

8bit DMA Bus

PDReq

PDAck

xPDWR, xPDRD

FIFO

SIE

UTM

DMA Interface

CPU Interface

8bit CPU Bus

Exclusive Bus Mode

General CPU/DMAC

Common Bus Mode

S1R72013

8bit DMA Bus

PDReq

PDAck

xPDWR, xPDRD

FIFO

SIE

UTM

DMA Interface

CPU Interface

CA

xCS

xWR, xRD

xCS

xWRH, xWRL

xRDH, xRDL

PDReq

PDAck

16bit Common Bus

USB Interface

EPSON

Rev.1.0
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